(Please write your Exam Roll No.)

Exam Roll No. 01250404415

END TERM EXAMINATION

FIRST SEMESTER [MCA] DECEMBER 2015- JANUARY 2016

Paper Code: MCA 107 **Subject: Computer Organization**

Time : 3 Hours **(Batch: 2015)**

Maximum Marks :75

Note: Attempt any five questions including Q.no.1 which is compulsory.

Q1. a) Which register keeps track of the instruction stored in program stored in Memory?
b) What is CSA? **(2.5x10=25)**
c) Differentiate a level triggered from a edge triggered flip-flop.
d) Which addressing mode used in an instruction of the form ADD R1 R2?
e) Distinguish between Array processing and Vector processing.
f) What are Hazards?
g) What is opcode?
h) Which kind of instruction changes the flow of program?
i) State hierarchy of memory of a computer system.
j) Suggest a solution to overcome the limitation on the speed of an adder.

Q2. a) Explain the operation of a JK master slave flipflop. **(6.25)**
b) Illustrate the working of a 4-bit bi-directional shift register. **(6.25)**

Q3. a) Write a note on register transfer language. **(6.25)**
b) Design a 4-bit combinational circuit decrementer using four full adder circuits. **(6.25)**

Q4. Define the following: **(12.5)**
a) microoperation b) microinstruction c) microprogram d) microcode

Q5. a) Show a circuit arrangement, whereby several devices may interrupt a processor on a single interrupt request line. **(6.25)**
b) Discuss various instruction formats. **(6.25)**

Q6. a) Draw a space time diagram for a six-segment pipeline showing the time it takes to process eight tasks. **(6.25)**
b) Distinguish between scalar RISC and superscalar RISC in terms of instruction issue, pipeline architecture and processor performance. **(6.25)**

Q7. a) Explain with examples, the various modes of data transfer. **(6.25)**
b) What is difference between isolated I/O and memory mapped I/O? State the advantages and disadvantages of each. **(6.25)**

Q8. a) How many 128x8 RAM chips to provide a memory capacity of 2KB? How many address line will be required to access the 2KB memory? How many lines must be decoded for chip select? Specify the size of decoders. **(6.25)**
b) Design an 8x8 Omega Network. **(6.25)**

Q9. Explain the following terms associated with cache design. **(6.25x2=12.5)**
a) Write through vs Write Back Caches
b) Cachable vs Non Cachable Data

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