(Please write your Exam Roll No.) *Exam Roll No. ……*

END TERM EXAMINATION

FIRST SEMESTER [MCA] DECEMBER-2012

Paper Code: MCA 107 *Subject: Computer Organisation*

Time : 3 Hours **Maximum Marks : 60**

Note : Attempt any five questions including Q. no. 1 which is compulsory.

Select one question from each unit.

Q1 Answer the following:- (2x10=20)

a) Define Control Word.
b) Differentiate SIPO and PIPO in shift registers.
c) Starting from an intitial value of R=11001101. Detremine the sequence of binary values in R, after logical shift-left,followed by a logical shift-right.
d) Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline.
e) Define Effective address.
f) What must the address field of an indexed addressing mode instruction be to make it the same as a register indirect mode instruction?
g) What is memory interleaving?
h) Explain the microinstruction format.
i) Define program status word.
j) What is universal shift register?

UNIT-1

Q2 (a) What are race conditions in flip=flop? Explain the J-K flip-flop. (5)

(b) Design and explain the 8:1 multiplexer. (5)

Q3 (a) What is register transfer language? Explain the arithmetic micro-operations. (5)

(b) Explain the applications of logic micro-operations. (5)

UNIT-II

Q4 (a) A computer uses a memory unit with 256K words of 32 bits each . A binary instruction code stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part. (5)

(i) How many bits are there in the operation code the register code part and the address part?
(ii) Draw the instruction word format and indicate the no. of bits in each part.
(iii) How many bits are there in the data and address inputs of the memory?

(b) How many types of control organizations are there? Discuss in brief. (5)

Q5 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400.A processor register R1 contains the number 200. (5)

Evaluate the effective address if the addressing mode of the instruction is-

(i) Direct ii) immediate iii) relative

(iv) register indirect (v) index with R1 as the index register.

(b) What is stack memory organization? Explain in brief. (5)

UNIT-III

Q6 (a) Formulate a six-segment instructions pipeline for a computer. Specify the operations to be performed in each operation (5)

(b) Give short notes on – (i) Priority interrupt (ii) DMA.

Q7 (a) Describe different types of modes of transfer. (5)

(b) Give short notes on – (i) Parallel processing (ii) Vector processing.

UNIT-IV

Q8 (a) What do you mean locality of reference? Discuss different mapping schemes of cache organization. (5)

(b) what is content addressable memory ? (5)

Q9 (a) Define the following – (5)

(i) Page fault and page replacement. (ii) Virtual memory

(b) what are multiprocessors ? Explain the characteristics of multiprocessors. (5)

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