(Please write you Exam Roll No.) Exam Roll No. ……..

END TERM EXAMINATION

FIRST SEMESTER [MCA] JANUARY 2011

Paper Code: MCA107	**Subject: Computer Organization (Batch: 2010)**
Time: 3 Hours	**Maximum Marks: 60**

Note: Q. no. 1 is compulsory. Attempt one question from each unit.

1. Compulsory Questions : **(10 x 2)**

i) Explain SIMD array processor.
ii) What is the advantage of having independent set of conditional codes ?
iii) What is monitor program?
iv) What is the head of a disk ?
v) Which industry is the primary user of MICR ?
vi) What prevents RISC pipeline to achieve maximum speed?
vii) Register A holds the 8-bit binary 11011001.Determine the B operand and the Logic micro-operation to be performed in order to change the value of A to 01101101 ?
viii) Change (A+B)*C in reverse Polish notation ?
ix) Determine the number of clocks cycles that it takes to process 200 tasks in a six segment pipeline ?
x) What is priority interrupt ?
xi) What is FIFO buffer ?

UNIT – I

2. **(a)** How a subroutine call is different from branching ? **3**

(b) A digital system has 16 registers,each with 32 bits.it is necessary to provide parallel data transfer from each register to every other register. **7**

i) How many lines are needed for transfer along 4 common bus ?
ii) How many lines are needed for direct parallel transfer ?
iii) If the registers form a scratch-pad memory,how is information transferred from one register to another? Let the register in the memory be designated as R0 TO R15.
iv) List the sequence of micro operations for a transfer of contents R6 to R13.

OR

3. (a) Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable and one 2-to-4 line decoder ? **3**

(b) Discuss the race round condition in J-K flip flop. **2**

c) Briefly describe the various categories of instructions in a general purpose microprocessor.Suppose that you have to design the instruction set architecture for a special purpose microprocessor that carries out basic graphic functions,what extra instruction(s) and register(s) would you suggest ? **5**

UNIT II

4. What are the typical applications and limitation of **3**

(a) (i) Relative addressing mode.

(ii) Based, indexed addressing mode.

(b) A program contains 1000 machine instructions.These are executed in a 7 stage instruction pipeline.Due to various data dependencies,10 cycles are wasted for every batch of 50 instructions.Branch instructions cause a further wastage of 20% extra cycles.Calculate the speed up of the pipeline as compared to a non-pipeline processor. **7**

OR

5. Define the following:- **5**

a) i) Micro instruction

ii) Micro program

iii) Control Memory

b) Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operation for evaluating the numerical result. **5**

(3+4)[10(2+6)+8]

UNIT – III

6. A 512-bits data packet needs to be prepared with 16-bit words,for serial asynchronous communication.There is 1 start bit and 1.5 stop bits for each word.The data packet is then encapsulated with 8-bit SOH,8 bit ETX and 16 bit CRC.Calculate the total overhead (in percentage) of transferring 1000 such packets. **10**

OR

7. i) What are four different types of pipelining ? **10**

ii) Using Booths algorithm,illustrate the sequence of steps in a tabular fashion ,when 11101 is multiplied with 10111.

UNIT-IV

8. A computer system needs 2 KB of RAM,2KB of ROM and 3 I/O ports with 3 registers in each.The first 1 KB of memory space is occupied by ROM and finally the I/O port addresses.To construct this memory system 512 x 8 RAM chips are used.Show the complete map of the system. **10**

OR

9. Write short notes on any **five** from followings:- **10**

(i) Cache memory
(ii) Virtual memory
(iii) Memory management hardware
(iv) CACHE COHERENCE
(v) SEMAPHORE AND its TSI instructions
(vi) Parallel computing

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