(Please write your Roll No. immediately) **Roll No. ……**

End-Term Examination

Second Semester [MCA] – MAY-JUNE 2006

Paper Code: MCA-106 **Subject: Computer System Architecture**
Paper ID : 44106

Time: 3 Hours **Maximum Marks: 60**

Note: Attempt any six questions including Q. 1 which is compulsory. All question carry equal marks

Q. 1 Attempt all parts :- **(1 x 10 = 10)**

(a) Name a computer machine that combines several instructions into a single instruction.
(b) What is the memory addressing capability of a microprocessor which has 24 address pins?
(c) What is the advantage of having independent set of conditional codes?
(d) What is a monitor program?
(e) What is the head of a disk?
(f) Which industry is the primary user of MICR (Magnetic Inc Character Recognition)?
(g) What prevents RISC pipeline to achieve maximum speed?
(h) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value of A to 01101101?
(i) Change (A+B)*C in reverse Polish notation?
(j) Determine the number of clocks cycles that it takes to process 200 tasks in a sig-segment pipeline?

Q. 2

(a) What is difference between instruction stream and data stream? **(2)**
(b) Find out the average access time for a fixed head disk rotating at 300 rpm and contains 10 sectors in a track? **(3)**
(c) What is the difference between logical shift, circular shift and arithmetic shift. Give suitable examples? **(5)**

Q. 3

(a) What are the differences between external and internal interrupts? **(3)**
(b) Define the term Program Status Word. **(2)**
(c) Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive-NOR, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage? **(5)**

Q. 4

(a) What are the differences between Static Memory and Dynamic Memory? **(2)**
(b) What are four different types of pipelining? **(2)**
(c) Draw the flowchart for multiplying two floating point numbers? **(6)**

Q. 5

(a) How a subroutine call is different from branching? **(2)**
(b) Construct a 5-to-32 line decoder with four 3-to-8-line decoders with enable and one 2-to-4-line decoder? **(8)**

Q. 6

(a) If the program counter is always one count ahead of the memory location from which the machine code is being fetched, how does the micro-processor change the sequence of program execution with a jump instruction? **(3)**
(b) Formulate a mapping procedure that provides eight consecutive micro instructions for each routine. The operation code has six bits and the control memory has 2048 words? **(3)**
(c) Compare the RISC and CISC architecture? **(4)**

Q. 7

(a) A 36-bit floating point binary number has eight bits plus sign for the exponent and 26 bits plus sign for its mantissa. The mantissa is a normalized fraction. Numbers in the mantissa and exponent are in signed magnitude representation. What are the largest and smallest positive quantities that can be represented, excluding zero? **(4)**
(b) Explain the difference between hardwired control and micro-programmed control. Is it possible to have a hardwired control associated with a control memory? **(6)**

Q. 8 Write short notes on any two:- **(5 x 2 = 10)**

(a) RS 232 C protocol
(b) Associative Memory
(c) IBM PC bus.

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End-Term Examination

Second Semester [MCA] – MAY 2005

Paper Code: MCA-106 **Subject: Computer System Architecture**

Time: 3 Hours **Maximum Marks: 60**

Note: Q. 1 is compulsory. Other questions have two alternative to choose from.

Q. 9 Justify or refute the following statement clearly, citing examples whether possible.

(a) A combinational shifter is less efficient as compared with a sequential shifter, as it requires extra multiplexers. 3

(b) Indirect addressing usually reduces the amount of assembly code for a given program, as compared to direct addressing. 3

(c) Since the "Interrupt Enable" (IEN) is disabled automatically during an interrupt cycle if a pending interrupt is deleted, therefore no further interrupt can be served while executing the ISR. 3

(d) Since associative caches are addressed by content, there is no need for separate address lines to access individual locations of the caches, as in RAM. 3

(e) The burst mode of DMA transfer is more efficient for data transfers to / from magnetic disks but rather inefficient for data transfer to / from magnetic tapes. 3

(f) Code written in RTL helps us to design digital systems systematically. 3

(g) An array multiplier's speed is bottlenecked by the same time taken to add the partial operand together. 2

UNIT -1

Q. 10 Alternate 1:-

(a) An atomic (or indivisible) memory operation comprises a memory read, modify and a memory write operations in an unbroken sequence. Show the micro operations in an unbroken sequence. Show the micro operations to carry out this read modify write cycle. Also, draw a schematic showing the hardware components to carry out this memory operation. 6

(b) Briefly describe the various categories of instructions in a general purpose microprocessor. Suppose that you have to design the instruction set architecture for a special purpose microprocessor that carries out basic graphic functions, what extra instruction(s) and register(s) would you suggest? 4

(OR)

Alternate 2:-

(a) A microprocessor checks its INTR line during the last clock cycle of each instruction cycle, and sets a flag R if there is a pending interrupt. In the first clock cycle of the current instruction, if R is high, the processor output INTA and checks bits b2, b3, b4 of its data bus. If then stores a 32 bit return address in a byte addressable memory at a location which is 8x (b4b3b2) and jumps to the next location. Illustrate the sequence of events during the interrupt cycle with a flow chart. 5

(b) Briefly outline the working of a two pass assembler, indicating the core steps and outputs generated during each pass. 5

UNIT -2

Q. 11 Alternate 1:-

(a) Describe the typical format of a vertically encoded microinstruction. Write the "Fetch" routine and the "execute" routine for the LOAD microinstruction. Assume a microprocessor with an accumulator, other basic registers and 2-operand format. You may use symbolic forms of the micro-operations needed. 6

(b) What are the typical applications and the limitation of (i) Relative addressing mode (ii) Based, indexed addressing mode. 4

Alternate -2 :-

(a) "Today; traditionally CISC microprocessors employ RISC characteristics, whereas RISC microprocessor employ CISC characteristics". Explain this comment with illustrative examples. 5

(b) A program contains 1000 machine instructions. These are executed in a 7 stage instruction pipeline. Due to various data dependencies, 10 cycles are wasted for every batch of 50 instructions. Branch instructions cause a further wastage of 20% extra cycles. Calculate the speed up of the pipeline as compared to a non-pipeline processor. 5

UNIT -3

Q. 12 Alternate 1 :-

(a) A microprocessor multiplexes data from four different data terminals, and sends the multiplexed data over a telephone link to a remote unit, via a UART. Suggest the most suitable I/O communication scheme (such as parallel, serial, synchronous, asynchronous, strobed, handshaked) between :

(i) The data terminals and the microprocessor
(ii) The microprocessor and the UART.
(iii) The UART and the remote unit 5

(b) Using Booths algorithm, illustrate the sequence of steps in a tabular fashion, when 11101 is multiplied with 10111. 5

Alternate 2:-

(a) A 512-bits data packet needs to be prepared with 16-bit words, for serial asynchronous communication. There is 1 start bit and 1.5 stop bits for each word. The data packet is then encapsulated with an 8-bit SOH, 8 bit ETX and 16 bit CRC. Calculate the total overhead (in percentage) of transferring 1000 such packets. 5

(b) Draw a flow chart showing the steps of floating point addition. Illustrate the sequence of steps with the binary equivalents of 0.34375 and 0.125, stored in their normalized forms. 5

UNIT -4

Q. 13 Alternate 1:-

(a) Compare the direct mapped cache system with the associatively mapped cached system in terms of design, flexibility, cost, replacement technique and impact on hit ratio. 5

(b) A magnetic disk has the following characteristics: 5

- Seek time to reach 0^{th} (outermost) track = 8 ms and seek time to reach 300^{th} (inner most) track =14 ms. Assume a linearly increasing seek time within this interval.
- Rotational speed = 3600 rpm
- Number of bits per track = 4096
- No. of bits per sector = 512

Calculate the time taken to read a 32 K bits file that starts on the 3^{rd} sector of the 200^{th} track.
Assume the average rotational latency to locate the first sector. i.e. start of file.

Alternate 2:-

(a) Enumerate some requirements which are needed specially for multiprocessor system from the viewpoint of memory processor failures, communication and software. 6

(b) A computer system needs 2 KB of RAM, 2KB of ROM and 3 I/O ports with 3 registers in each. The first 1 KB of memory space is occupied by ROM and finally the I/O port addresses. To construct this memory system 512 x 8 RAM chips are used. Show the complete memory map of the system. 4

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End-Term Examination

Second Semester [MCA] – MAY 2004

Paper Code: MCA-106 **Subject: Computer System Architecture**

Time: 3 Hours **Maximum Marks: 60**

Note: Attempt any five questions.

Q. 1 A digital system has 16 registers, each with 32 bits. It is necessary to provide parallel data transfer from each register to every other register.

(a) How many lines are needed for transfer along 4 common bus? 3

(b) How many lines are needed for direct parallel transfer? 3

(c) If the registers from a scratch–pad memory, how is information transferred from one register to other? Let the register in the memory be designated as R_0 to R_{15} 6

List the sequence of micro operations for a transfer of contents of R_6 to R_{13} .

Q. 2 (a) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with one enable and one 2-to-4-line decoder. 8

(c) Obtain the 10's complement of the following six digit decimal number :

123900, 090 657, 100000, 000000. 4

Q. 3 (a) A sequential circuit has two D flip-flop A and B, two inputs X and Y and one output Z. The flip-flop input equations and the circuit output are as follows :-

$D_A = XY + XA$, $D_B = X^1B + XA$, $Z=B$

(i) Draw the logic diagram of the circuit.

(ii) Tabulate the state table. 8

(b) Discuss race around conditions in J-K flip-flop. 4

Q. 4 (a) Define the following:- 6

(i) Micro instruction

(ii) Micro Program

(iii) Control Memory

(b) Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operation for evaluating the numerical result.

(3+4) [10(2+6) + 8] 6

Q. 5 (a) What is the difference between RISC and CISC processors? 6

(b) Draw the flowchart for multiplying two floating point-numbers. 6

Q. 6	Explain the following :- (a) Vector processor. (b) Associative Memories	12
Q. 7	Explain following: - (a) Modes of data transfer (b) Input/ output processor	12
Q. 8	Write short notes on any two :- (a) Cache memory (b) Virtual memory (c) Memory management hardware	12

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End-Term Examination

Second Semester [MCA] – MAY 2003

Paper Code: MCA-106 **Subject: Computer System Architecture**

Time: 3 Hours **Maximum Marks: 60**

Note: Attempt any five questions.

Q. 1 (a) What is De-Multiplexer? How can you make decoder to function as a De-multiplexes? Show this by a block diagram and truth table. 5

(b) Given a 32 x 8 ROM chip with an enable input, show the external connection necessary to construct 128 x 8 ROM with four chips and a decoder. 7

Q. 2 (a) If we need to link 16 registers to a common bus, when each register is 32-bit then, 6

(i) How many multiplexer will be required?

(ii) How many input lines are required for each multiplexer? This should also include adequate number of selection lines.

(b) Register A holds the 8-bit binary 11011001, determine the B operand and the logic micro-operation to be performed in order to change the value in A to

(i) 01101101 (ii) 11111101. 6

Q. 3 (a) With the help of flow chart, explain the sequence of steps for an instruction cycle. How does an interrupt change the sequence of events? 6

(b) Give the schematic diagram of a micro program sequence and briefly explain functions of its different components. 6

Q. 4 (a) Convert the following numerical arithmetic expressions into reverse polish notation and show the stock operations for evaluating the results. 6

(3+4) [10 (2+6) + 8]

(b) What do you understand by "Reduced instruction set computer" (RISC), How are they differ from CISC. 3

(c) What is difference between direct addressing mode and indexed addressing mode instruction. 3

Q. 5 (a) Discuss the application of pipelines, illustrate through a system having 4 segment instruction pipelines. Also discuss what is speed up in a pipeline architecture. 5

(b) Calculate the speed up in case of a computer with four floating-point pipeline processors. Each processor uses a cycle time of 40 μs. Total number of floating point operation to be made is 400. 5

(c) Differentiate between supercomputer & Multi-computers 2

Q. 6 (a) Explain Booth's algorithm for multiplication. Give the schematic diagram of the hardware needed to implement Booth's algorithm. Depict the algorithm using the hardware through a flow chart's what happens when there is an overflow? 6

(b) A 48 bit computer stores floating point number is sign-magnitude form with 12 bits for exponent (including sign bit). Find the range of numbers that can be represented on this computer. 6

Q. 7 (a) What is I/O processor and what are its functions & advantages? Also discuss how I/O interrupts make more efficient use of CPU. 6

(b) In case of Direct-mapping cache & Fully associated Cache and considering their merits discuss / answer the following; 6
(i) rank these in terms of hardware complexity & implementation cost.
(ii) With each cache organization, what is the effect of block-mapping policies on the hit-issue ratio.

Q. 8 Write short note on any three:- 3 x 4

(a) Hardwired control and micro-program control
(b) Virtual memory concept.
(c) Overlapped Register windows
(d) Arithmetic pipeline
(e) SIMD array processor.

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End-Term Examination

Second Semester [MCA] – JUNE 2001

Paper Code: MCA-106 **Subject: Computer System Architecture**

Time: 3 Hours **Maximum Marks: 70**

Note: Attempt any five questions.

Q. 1 (a) A sequential circuit has two D-flip-flop A and B, two inputs x and y and one output Z. The flip-flop input equations and the circuit output are as follows : 8

$D_A = x' y + xy$, $D_B = x'B + XA$

$Z = B$

(i) Draw the logic diagram of the circuit.

(ii) Tabulate the state table.

(b) Construct a 5 to 32 line decoder with four 3 to 8 line decoders with enable and one 2 to 4 line decoder. 6

Q. 2 (a) Draw the logic diagram of basic computer registers connected to a common bus. 4

(b) Draw the instruction code formats of the basic computer. 4

(c) Draw the flowchart of computer cycles. 6

Q. 3 (a) Design a 4 bit decrementer circuit using four full adder circuits. 7

(b) Design an arithmetic circuit with on selection variable S and two n- bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for first two stages. 7

S	Cin	Cin = 1
0	D= A+B	D=A+1
1	D=A-1	$D=A + \overline{B} + 1$

Q. 4 (a) An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow. 5

(b) Write short note on stack organization. 5

(c) Discuss the use of Register transfer language. 4

Q. 5 (a) What is parallel processing? Discuss various types of parallel processing techniques. 6

(b) Discuss addressing modes with examples. 6

(c) Write short note on micro-programmed control unit. 4

Q. 6 (a) Show the contents of registers E, A, Q and SC during the process of multiplication of two binary numbers, 11111 (multiplicand) and 10101 (multiplier). 5

(b) Draw the flow chart for multiplication algorithm. 5

(c) Show that adding B after the operation A + $\overline{B}$ + 1 restores the original value of A. What should be done with the end carry? 4

Q. 7 (a) Design parallel priority interrupt hardware with S-interrupt sources. 6

(b) Discuss the DMA transfer in a computer system using block diagram. 4

(c) What is the basic advantage of using interrupt initiated transfer over transfer under program control without an interrupt. 4

Q. 8 (a) A computer employs RAM chops of 256 x 8 and ROM chips of 1024 x 8. The Computer system needs 2K bytes of RAM, 4K bytes of RAOM, and four interface units, each with four registers. A memory mapped I/O organization is used. The two highest order bits of the address bus are assigned 00 of RAM, 01 of ROM, and 10 for interface registers. 10

(a) How many RAM and ROM Chips are needed?
(b) Draw a memory address map.
(c) Give address range in hexadecimal for RAM, ROM and interface.

(b) Write short note on cache memory. 4

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End-Term Examination

Second Semester [MCA] – AUGUST 2000

Paper Code: MCA-106	**Subject: Computer System Architecture**

Time: 3 Hours **Maximum Marks: 70**

Note: Attempt seven questions in all. Out of these, three each should be from Sec-1 and Section- B.

SECTION-A

Q. 1 (a) Given a 32 x 8 ROM chip with an enable input show the external connection necessary to construct a 128 x 8 ROM with four chips and a decoder. 5

(b) What is the difference between following CPU organization. 5

(i) Single accumulator organization.
(ii) General Register organization
(iii) Stack Organization

Q. 2 (a) What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt? 2

(b) Explain in details Daisy Chain priority interrupt Scheme. 8

Q. 3 (a) Draw the flow chart for multiplying two floating point numbers. 5

(b) What is the difference between isolated I/O and memory mapped I/O? What are advantages and disadvantages of each. 5

Q. 4 (a) The content of the top of a memory stack is 5320. The content of the stack Pointer SP is 3560. A two word call subroutine instruction is located in memory at address 1120 followed by the address of the field of 6720 at location 1121. What are content of PC, SP and top of stack: 3

(i) Before the call instruction is fetched from memory.
(ii) After the CALL inst. is executed.
(iii)After the return from subroutine.

(b) Convert the flowing arithmetic expression into postfix notation and show the stack operations for evaluating the numerical result. 3

(4+9)(10(3+9) + 6)

(c) What is the difference between logical, circular and arithmetic shift. 4

Q. 5 What do you mean by Cache memory? Explain in detail mapping procedures used while considering organization of Cache Memory. 10

SECTION-B

Q. 6 A computer has following registers PC(12 bits), MAR(16), MBR(12), I(1), OPR(3), E(1), AC(16) and six timing signal t_0 to t_5 and one flip-flop F for cycle control. Fetch cycle is performed when F=0 and execute cycle when F=1. List the micro-operations and control functions for the computer 10

(i) When F=0

(ii) For Executing XOR, SWAP (AC and memory Word) ADD (M← M+AC)

Q. 7 (a) How many characters per second can be transmitted over a 1200 baud line in each of following models? (Assume a character code of 8 bits) 3

(i) Synchronous Serial transmission

(ii) Asynchronous serial transmission with two stop bits.

(iii) Asynchronous serial transmission with one stop bit.

(b) Write a short note on input output processor. 7

Q. 8 (a) Draw and explain the block diagram of DMA controller. Why Read and Write lines of a DMA controller are bi-directional. 5

(b) A two-way set associative Cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K x 32. What are sizes of

(i) TAG (ii) Index (iii) Data (iv) Cache Memory 5

Q. 9 What do you mean by RISC pipeline? Specify pipelining configuration for three segment instruction pipeline. 10

Q. 10 Write short notes on any two of the following: 10

(a) SIMD array processor

(b) FIFO Buffer

(c) Virtual Memory.
