(Please write your Exam Roll No.) Exam Roll No. ……..

End Term Examination

Second Semester [MCA] MAY-JUNE 2009

Paper Code: MCA – 106	**Subject: Computer System Architecture**
Paper ID: 44106	**(Batch 2004 – 2008)**
Time : 3 Hours	**Maximum Marks : 60**
Note: Q1. is compulsory. Attempt four questions from the rest.	

Q1. Answer the following questions.

a) A weather forecasting computation requires 250 billion floating point operations. The problem is possessed in a supercomputer that can perform 100 megaflops. How long it would it would take to do these computations? **(3)**

b) "Today; traditionally CISC microprocessors employ RISC characteristics, whereas RISC microprocessors employ CISC characteristics". Explain briefly this comment with illustrative examples. **(3)**

c) What is the purpose of snoopy-bus protocol? **(2)**

d) Comment on "Interrupt Enable (IEN) is disabled automatically during an interrupt cycle if a pending interrupt is deleted, therefore no further interrupt can be served while executing the ISR". **(3)**

e) Explain operand forwarding. **(1)**

f) Explain arithmetic and instruction pipelining. **(2)**

g) What is the objective of cycle stealing in DMA? **(1)**

h) Explain multi-port memory. **(1)**

i) Explain hand shaking process in asynchronous transmission. **(2)**

j) Explain relevance of memory interleaving in pipelining/vector processing. **(2)**

Q2.

a) Draw flowchart of Booth multiplication algorithm. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 5-bit register that hold signed number.
(-15) x (-13) **(5)**

b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ration of the pipeline for 100 taskes. What is the maximum speedup that can be achieved? **(5)**

Q3.

a) A computer system needs 2 KB of RAM, 2KB of ROM and 3 I/O ports with 3 registers in each. The first 1 KB of memory space is occupied by ROM and finally the I/O port addresses. To construct this memory system 512 x 8 RAM chips are used. Show the complete memory map of the system. **(5)**

b) Main memory M1 and disk memory M2 constitute two level hierarchy virtual memory system that contains page frames as follows:
M1 page frame: a, b, c
M2 page frame: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
The CPU is generating page request in a sequence as 0, 1, 2, 4, 2, 3, 7, 2, 1, 3 and 1. by employing LRU,OPT and FIFO page replacement policies, find out the following(s).
   1. hit ratio for each policy **(4)**
   2. which one produces best result. **(1)**

Q4.

a) A 512-bits data packet needs to be prepared with 16-bit words, for serial asynchronous communication. There us 1 start bit and 1.5 stop bits for each word. The data packet is then encapsulate with an 8-bit SOH, 8 bit ETX and 16-bit CRC. Calculate the total overhead(in percentage) of transferring 1000 such packets. **(5)**

b) Draw a flow chart showing the steps of floating point addition. Illustrate the sequence of steps with the binary equivalents of 0.34375 and 0.125, stored in their normalized forms. **(5)**

Q5

a) What are the typical applications and the limitation of (i) Relative addressing mode (ii) Based, indexed addressing mode. **(5)**

b) A microprocessor multiplexes data from four different data terminals, and sends the multiplexed data over a telephone link to a remote unit, via a UART. Suggest the most suitable I/O communication scheme (such as parallel, serial, synchronous, asynchronous, strobed, handshaked) between: **(5)**

   i. The data terminals and the microprocessor
   ii. The microprocessor and the UART
   iii. The UART and the remote unit.

Q6.

a) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with one enable and one 2-to-4-line decoder. **(5)**

b) Obtain the 10's complement of the following sin digit decimal number:
123900, 090657, 100000, 000000 **(5)**

Q7.

a) Explain Instruction cycle and Interrupt cycle with the help of flowchart. Describe instruction format and addressing mode bits. **(5)**

b) Explain the architecture of content Addressable Memories and logic for searching particular word in the memory. **(5)**

Q8. write short notes on **<u>any five:-</u>** **(2x5 = 10)**

a) Cache memory
b) Virtual memory
c) Memory management hardware
d) Vector processor
e) Micro instruction
f) Micro program
g) Control Memory

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