(Please write your Exam. Roll No.) Exam. Roll No. 0312149259

END TERM EXAMINATION

THIRD SEMESTER (BCA), DECEMBER - 2010

Paper Code : BCA - 203	*Subject : Computer Architecture*
Paper ID : 20203	

Time : 3 Hours *Maximum Marks : 75*

Note : Q. 1 is compulsory. Attempt One question from each unit.

Q. 1. (a) Design a 4-bit combinational circuit decrementer using four full-adder circuits. (5)

(b) Explain interrupt cycle with an example. (5)

(c) What is an Input-Output interface? Why is it needed? (5)

(d) Explain the concept of virtual memory. How is it implemented? (5)

(e) What is associative memory? Explain its architecture. (5)

UNIT - I

Q. 2. (a) Describe Basic Instruction Set. Is it complete? Justify. (8·5)

(b) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value in A to : (4)

(i) 01101101

(ii) 11111101

Q. 3. (a) Draw a diagram of bus system for four registers with 8-bit each using three-state buffers and decoder. (6·5)

(b) Explain hard wired control unit organisation. (6)

P.T.O.

UNIT - II

Q. 4. (a) Show the contents in hexadecimal of registers PC, AR, DR, IR and SC of the basic computer when an ISZ indirect instruction is fetched from memory and executed. The initial content of PC is 7FF. The content of memory at address 7FF is EA9F. The content of memory at address A9F is 0C35. The content of memory at address C35 is FFFF. (5)

(b) Convert the following arithmetic expressions from infix to reverse Polish notation :

$A + B * [C * D + E * (F + G)]$ (4·5)

(c) Give three examples each of external and internal interrupts. (3)

Q. 5. (a) Write a program to evaluate the arithmetic statement :

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$

(i) Using a general register computer with one-address instructions.

(ii) Using a stock organised computer with zero-address operation instructions. (8)

(b) The content of PC in the basic computer is 3AF. The content of AC is 7EC3, The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. What is the instruction that will be fetched and executed next? (4·5)

UNIT - III

Q. 6. (a) Describe the algorithm for division of two fixed-point binary numbers in signed-magnitude representation. (6·5)

(b) Draw the block diagram of DMA contorller. Also explain DMA transfer in computer system. (6)

Q. 7. (a) Design a parallel priority interrupt hardware for a system with eight interrupt sources. (6)

(b) Discuss handshaking approach for asynchronous data transfer. (6·5)

UNIT - IV

Q. 8. (a) Construct a 4096 × 8 main memory with 2048 bytes each of RAM and ROM using 128 × 8 RAM chips and 512 × 8 ROM chips. List also the memory address map. (7·5)

(b) Describe memory hierarchy in computer system. (5)

Q. 9. (a) Consider the following page reference stream :

1, 2, 3, 4, 5, 6, 2, 1, 2, 3, 5, 6, 3, 2, 4, 2, 6.

If a process is allocated four frames, how many page faults would occur if page replacements are done using the

(i) FIFO

(ii) LRU (8)

(b) The logical address space in a computer system consists of 128 segments. Each segment can have upto 32 pages of 4K words in each. Physical memory consists of 4K blocks of 4K words in each. Formulate the logical and physical address formats. (4·5)

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