END TERM EXAMINATION

THIRD SEMESTER [BCA] DECEMBER-2009

Paper Code: BCA203	**Subject: Computer Architecture**
Paper Id-20203	

Time : 3 Hours	Maximum Marks :75

Note: Q.1 is compulsory. Attempt one question from each unit.

Q1   Attempt **any ten** from the following:-   **(10x2.5=25)**

(a) Draw the block diagram for the hardware that implements the following statements: x+yz : AR←AR+BR., where AR and BR are two n-bit registers and x, y and z are control variables.

(b) Design a 4-bit combinational circuit decrementer using four full adders.

(c) What are the two instructions needed in the basic computer in order to set the E flip flop to 1?

(d) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part. Draw the instruction word format and indicate the number of bits in each part.

(e) Write any three functions of stack.

(f) Why does DMA have priority over CPU when both request a memory transfer?

(g) Define overflow. How can we detect overflow?

(h) Give two advantages of booth multiplication.

(i) List various resistors with their functions required for basic computer function.

(j) (i) How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(ii) How many lines of address bus must be used to access 2048 bytes of memory?

(k) A ROM chip of 1024x8 bits has four select inputs and operates from a 5-volt power supply. How many pins are needed for the IC package? Draw a block diagram and label all input and output terminals in the ROM.

(l) Define hit ratio.

UNIT-I

Q2   (a) Tabulate various shift micro operations and design a 4 bit combination circuit shifter.   **(5)**

(b) The output of four registers R0, R1, R2, R3 are connected through 4-to-1-line multiplexers to the inputs of a fifth register, R5. Each register is eight bits longs. The required transfers are dictated by four timing variables T_0 through T_3 as follows:

T_0 :   R5←R0

T_1 :   R5←R1

T_2 :   R5←R2

T_3 :   R5←R3

Timing variables are mutually exclusive. Draw a block diagram showing the hardware implementation of the register transfers.   **(5)**

(c) Starting from an initial value of R=11011101, determine the sequence of binary values in R after a logical shift-left followed by a shift-right and a circular shift-left.   **(2.5)**

P.T.O.

Q3 (a) Describe the hardware implementation of logic micro operation. Draw the diagram of one stage of logic circuit used with AND, OR, NAND and XOR gates. **(5)**

(b) What is the difference between a direct and indirect address instruction? **(5)**

(c) Give a suitable example to discuss insert operation. **(2.5)**

UNIT-II

Q4 (a) Design a flow chart showing instruction cycle and interrupt cycle for basic computer operation. **(5)**

(b) Tabulate various memory reference instructions. Explain BUN and BSA. **(5)**

(c) Giving suitable block diagram show major components of CPU. **(2.5)**

Q5 (a) Illustrate the influence of number of address on $X=(R+S)(U+V)$ using three address, two address and zero address instruction. **(5)**

(b) What is stack organization? Describe its function using a suitable example. Define stack limit. **(5)**

(c) What is the difference between implied and immediate addressing modes? **(2.5)**

UNIT-III

Q6 (a) Design and discuss 2 bit by 3 bit array multiplier. Give its major advantages. **(5)**

(b) Taking multiplicand 11111 and multiplier 01001 design a table of multiplication with booth multiplication algorithm. **(5)**

(c) Give register configuration for hardware implementation of signed 2's compliment addition/subtraction. **(2.5)**

Q7 (a) What do you understand by hand shaking? Discuss using suitable diagram:
   (i) source initiated transfer using hand shaking.
   (ii) Destination initiated transfer using hand shaking. **(5)**

(b) What is priority? Name various types of priority. Discuss Daisy chaining priority in brief. **(5)**

(c) List four peripherals devices that produce an acceptable output for a person to understand. **(2.5)**

UNIT-IV

Q8 (a) What is mapping? Name various types of mapping. Discuss direct mapping in brief. **(5)**

(b) Write a short note on memory hierarchy. **(5)**

(c) A computer uses RAM chips of 1024x1 capacity. **(2.5)**
   (i) How many chips are needed to provide a memory capacity of 1024 bytes?
   (ii) How many chips are needed to provide a memory capacity of 16K bytes?

Q9 (a) Giving suitable block diagrams differentiate between RAM and ROM. **(5)**

(b) Write a short note on Auxiliary memory. **(5)**

(c) Draw a block diagram of Associative memory. **(2.5)**

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