(Please write your Exam Roll No.) Exam Roll No. 01314 22007

END TERM EXAMINATION

THIRD SEMESTER [BCA] DECEMBER-2008

Paper Code: BCA203 **Subject: Computer Architecture**
Paper Id: 20203 **(Batch: 2005-2007)**
Time : 3 Hours **Maximum Marks :75**

Note: Q.1 is compulsory. Attempt one question from each unit.

Q1 (a) What is wrong with the following register transfer statements? **(5)**

(i) $xT : AR \leftarrow \overline{AR},\ AR \leftarrow 0$ (ii) $yT : R1 \leftarrow R2,\ R1 \leftarrow R3$

(b) What do you understand by the branch and save return address? **(5)**

(c) Explain the Indexed addressing mode. **(5)**

(d) What is the difference between isolated I/O and memory mapped I/O? Also, explain the advantages and disadvantages of each. **(5)**

(e) What is memory hierarchy in a computer system? **(5)**

UNIT-I

Q2 (a) Starting from an initial value of R=11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left. **(4.5)**

(b) Design an arithmetic circuit with one selection variable S and two n-bit date inputs A and B. The circuit generates the following four arithmetic operation in conjunction will the input carry C_{in}. Draw the logic diagram for the first two stages. **(8)**

S	Cin=0	Cin=1
0	D=A+B	D=A+1
1	D=A-1	D=A+ $\overline{B}$ +1

Q3 (a) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? **(4.5)**

(b) Draw the block diagram of control unit of basic computer and explain. **(8)**

UNIT-II

Q4 (a) Draw full adder and explain its logic circuit. **(4.5)**

(b) What are the various phases of an instruction cycle? Give the microoperations of fetch and decode phases. How the first two register transfer statements are implemented? **(8)**

Q5 (a) What is the reverse polish notation? Explain with an example. **(4.5)**

(b) Write down a program to evaluate $Z = (A+B)*(C+D)*(G+H)$ by using three address instructions and zero address instructions. **(8)**

UNIT-III

Q6 (a) What do you understand by the divide overflow? **(4)**

(b) Show the contents of registers E, A, Q and SC during the process of multiplication of two binary numbers, 11111 (multiplicand) and 10101 (multiplier). The signs are not included. **(8.5)**

Q7 (a) Draw a block diagram for the DMA system showing the essential elements needed for the DMA transfer in a computer system. **(4.5)**

(b) Explain the difference between the daisy chaining priority and parallel priority interrupts. Draw the diagrams to explain their working. **(8)**

UNIT-IV

Q8 (a) Explain the concept of virtual memory. What are its advantages? **(4.5)**

(b) What is associative memory? Give and explain its architecture. **(8)**

Q9 (a) Explain the differences between cache and auxiliary memory. **(4.5)**

(b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is128Kx32. **(8)**

(i) Formulate all pertinent information required to construct the cache memory.

(ii) What is the size of the cache memory?

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