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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-JUNE 2009

Paper Code: BCA-106 *Subject: Digital Electronics*
Paper Id: 20106 *(Batch: 2005-2008)*
Time : 3 Hours *Maximum Marks :75*

Note: Q1. is compulsory. Attempt one question from each part.

Q1. (a) State and prove De-Morgan's theorem. **(5)**
(b) Describe and compare Register, Main Memory and Secondary Memory. **(5)**
(c) What are the drawbacks of S-R Flip-flop? How are they removed in J-K flip-flop? **(5)**
(d) Perform the following conversions: **(5)**
(i) $(AB.08)_{16} = (\quad)_{10}$
(ii) $(670.04)_8 = (\quad)_{16}$
(e) Design full-subtractor using NAND Gate only. **(5)**

PART-A

Q2. (a) Realize (i) $Y = A+BC\overline{D}$ using NOR Gates only. **(6)**
(ii) $Y = (A+C)(A+\overline{D})(A+B+\overline{C})$ using NAND Gates only.
(b) Express the function $Y = A+\overline{B}C+B\overline{D}$ in **(6.5)**
(i) Canonical SOP form
(ii) Canonical POS form

Q3. (a) Using the K-Map method, simplify the following Boolean function **(6.5)**
$F = \sum_m (0,2,3,6,7) + \sum_d (8, 10, 11, 15)$
And obtain (i) minimal SOP and (ii) minimal POS expressions
(b) If $\overline{A}B+C\overline{D}=0$, then by using Boolean algebra's laws and properties prove that: **(6)**
$AB + \overline{C}(\overline{A}+\overline{D}) = AB+BD+\overline{B}\,\overline{D}+\overline{A}\,\overline{C}\,D$

PART-B

Q4. (a) Explain Binary Multiplier. **(6)**
(b) Show how a full-adder can be converted to a full-subtractor with the addition of an inverter circuit. **(6.5)**

Q5. (a) What are MUX & DEMUX? Implement the following function using Multiplexer: **(6.5)**
$F=\sum_m(0,1,3,4,8,9,13,15)$
(b) Design a code converter to convert Grey code into Binary code. **(6)**

PART-C

Q6. (a) Define flip flop. Realize JK flip-flop using D-flip-flop. **(6)**
(b) Differentiate between combinational and sequential circuits. Explain the Race-Around condition and how can it be eliminated in Master-Slave JK Flip Flop? **(6.5)**

Q7. (a) What are shift Registers? How are they different from Data Registers? The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right with the serial input being 101101. What will be the final content of the register after all the 6 shifts are over? **(6.5)**
(b) Explain in detail the construction and working of Universal/Bidirectional shift register. **(6)**

PART-D

Q8. (a) Design a mod-10 counter to count in Grey code using D-flip flop. **(6)**
(b) What is a Ripple Counter? Draw the wave forms to explain how this circuit can be used as a "Frequency Divider". **(6.5)**

Q9. (a) What is a RAM? State the differences between Static RAM and Dynamic RAM. **(6)**
(b) What is a ROM? State the differences among ROM, PROM, EPROM and EEPROM. **(6.5)**

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