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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-2008

Paper Code:BCA-106 ***Subject: Digital Electronics***
Paper Id:20106 ***Batch (2005-2007)***

Time : 3 Hours ***Maximum Marks :75***

Note: Q1. is compulsory. Attempt one question from each part.

Q1. (a) State and explain the DeMorgan's theorem which convert a sum into a product form and vice-versa. **(5)**

(b) Design a full adder circuit using only NOR gates. What relations has it to the half-adder circuit. **(5)**

(c) What is a demultiplexer? Explain the difference between a DEMUX and MUX. **(5)**

(d) Discuss the difference between combinational and sequential logic. **(5)**

(e) Why are shift registers considered to be basic memory devices? **(5)**

PART-A

Q2. (a) Express the function $Y = A + \overline{B}\,C$ in (a) Canonical SOP and (b) Canonical POS form. **(12.5)**

(b) Explain the terms: (i) prime implicant (ii) input variable (iii) minterm and (iv) maxterm

Q3. (a) Realise (i) $Y = A + BC\overline{D}$ using NAND gates and **(12.5)**
(ii) $Y = (A + C)(A + \overline{D})(A + B + \overline{C})$ using NOR gates

(b) Realise the following function using (i) multilevel NAND-NAND network and (ii) multilevel NOR-NOR network.
$Y = \overline{A}B + B(C + \overline{D}) + \overline{E}\overline{F}(\overline{B} + \overline{D})$

PART-B

Q4. (a) Show how a full adder can be converted to a full subtractor with the addition of an inverter circuit. **(12.5)**

(b) Explain (i) 1-to-8 demultiplexer (ii) 1-to-16 demultiplexer.

Q5. (a) Design a parallel binary multiplier that multiplies a 4-bit number $B=B_3B_2B_1B_0$ by a 3 bit number $A=A_2A_1A_0$ to form the product $C=C_6C_5C_4C_3C_2C_1C_0$. **(12.5)**

(b) Draw the logic diagram of IC74180 parity generator/checker and explain its operation with the help of a truth table.

PART-C

Q6. (a) Explain the function of a D flip-flop using a suitable diagram and discuss how it works as a latch? **(12.5)**

(b) Show that a J-K flip-flop can be converted to a D flip-flop with an inverter between the J and K inputs.

Q7. (a) Explain the operation of master-slave flip-flop and show how the race around condition is eliminated in it? **(12.5)**

(b) What is the major difference in the operation of edge-triggered flip-flops and master-slave flip-flops?

PART-D

Q8. (a) What is a ripple counter? What factors determine whether a counter operates as a count-up or count-down counter? **(12.5)**

(b) What is a modulus counter? Draw the logic diagram of a 4 bit binary ripple counter using flip-flops that trigger on the positive-edge transition.

Q9. (a) What is a ROM? Explain the terms: (a) Volatile memory (b) Non Volatile memory. **(12.5)**

(b) Describe and compare sequential access memories, random access memories and read only memories.

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