(Please write your Exam Roll No.) *Exam Roll No. ..*

END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY - JUNE 2007

Paper Code:BCA-106 ***Subject: Digital Electronics (2005 Batch)***

Time : 3 Hours ***Maximum Marks :75***

Note: Question No. 1 is compulsory. Attempt four questions from the remaining paper, selecting one question from each part.

Q1. (a) Find out the value of the following.
(i) $(11010010)_2 = (X)_8$ (1)
(ii) $(AB)_{16} = (X)_2$ (1)

(b) Fill in the blanks
(i) _____ gate does not take part in logical operation. (1)
(ii) The _____ and _____ gates are universal gates. (1)
(iii) The gate _____ generates transfer function of applied input. (1)

(c) Simplify the following Boolean function and draw logical circuit. (5)
$F(A, B, C, D) = \Sigma (0, 6, 8, 13, 14)$
$D(A, B, C, D) = \Sigma(2, 4, 10)$

(d) Design 3-bit binary counter using T flip-flop. (5)

(e) Sum of all minterms of a Boolean function of n variables is 1. Prove this statement for n=3. (5)

(f) Construct a master-slave flip-flop using two R-S flip-flops. (5)

PART-A

Q2. (a) Design a combinational circuit whose input is a three bit number and whose output is 2's complement of the number. (7)

(b) Explain why NOR and NAND gates are universal gates. (5.5)

OR

Q3. (a) Design a 4-bit binary to gray code converter. (7)

(b) Design a BCD to Excess-3 code converter with a BCD-to-Decimal decoder and four OR gates. (5.5)

PART-B

Q4. (a) Explain a parallel binary adder with the help of logical diagram and sum two binary numbers A = 1101 and B=1001 using parallel binary adder. (7)

(b) Explain a full adder circuit and construct it with the help of a 3 X 8 Decoder and two OR gates. (5.5)

OR

Q5. (a) Design sequential circuit for the following state table using 2-bit register and combinational gates. (7.5)

Present State		INPUT	NEXT STATE	
A	B	X	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

(b) Construct a half Adder circuit using basic gates (AND, OR, NOT) only. (5)

PART-C

Q6. (a) A flip-flop has 20-ns delay from the time its CP input goes from 1 to 0 to the time the output is complemented. Find out the followings. (5)

(i) What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops?

(ii) What is the maximum frequency at which the counter can operate reliably?

(b) Explain shift register and different configurations of shift register. (7.5)

OR

Q7. (a) Why J-K flip-flops is known as universal flip-flop. Design a T-flip-flop and D-flip-flop using J-K flip-flop. (7)

(b) Design a logical diagram of a 32 x 4 ROM. (5.5)

PART-D

Q8. (a) Explain look-ahead carry generator and design logical diagram of a look-ahead carry generator. (7.5)

(b) Explain multiplexer and implement it to the following Boolean function using 4 x 1 multiplexer. (5)

$F(A, B, C) = \Sigma (1, 3, 5, 6)$

OR

Q9. (a) Design a combinational circuit that accepts a two bit number and generates a binary number equal to the square of the input number. (7.5)

(b) Write short notes on any two of the followings. (5)

(i) Encoder

(ii) Sequential Circuit

(iii) Edge-Triggered-Flip-Flop

(iv) Demultiplexers

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