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END TERM EXAMINATION

FIRST SEMESTER [MCA] DECEMBER-2008

Paper Code: MCA 103	**Subject: Digital Electronics**
Paper Id: 44103	**(Batch: 2004-2008)**

Time: 3 Hours **Maximum Marks: 60**

Note: Q. 1 is compulsory. Attempt one question from each unit.

Q.1 Answer the following:

(a) A NOR gate is also referred to as a 'Negative AND gate'. Why? (1)

(b) Give the maximum positive and negative numbers which can be represented in 2's complement form using n bits? (1)

(c) Most PC-compatible computer system use 20-bit address code to identify over one million binary locations. How many hex-characters are required to identify the address (1)

(d) The logic expression Y = ΠM(1,4,6,9,10,11,14,15) is equivalent to___ (1)

(e) How many states does a twisted ring counter consists of four flip-flops have? (1)

(f) Name three major categories into which programmable ROMs can be divided. (1)

(g) How does a priority encoder differ from an ordinary encoder? (1)

(h) What do you understand by system bus? (1)

(i) Why should the shift register stages be edge triggered? (1)

(j) Design a mod-3 binary counter? (2)

(K) Attempt **Any Three** of the following: (3 x 3 =9)

(i) Explain the operation of Schmitt Trigger work?

(ii) Obtain the canonical sum of product and product of sum of the following expression f = $X_1 X_2 X_3 + X_1 X_3 X_4 + X_1 X_2 X_4$

(iii) Design a 64: 1multiplexer using 16: 1multiplevers.

(iv) Design a parity checker circuit to add an even parity bit to a 16-bit word. Use two 74180 packages.

UNIT - I

Q2. (a) Discuss the advantages of digital system over analog system. What is the limitation of a digital system? (3)

(b) Convert the decimal numbers 95.5 into hexadecimal number. (2)

(c) Write the next four numbers in the following sequence (2)

(i) Octal counting sequence 124, 125, 126

(ii) Hexadecimal sequence E9A, E9B, E9C, E9D

(d) 7-bit hamming code is received as 1101101. Locate the error position and find the correct code. (2)

(e) What is the cyclic code? (1)

OR

Q3. (a) Add the following numbers using the 2's complement method 47 and

+29. (3)

(b) What is the necessary condition for a weighted code to be self-complementing code? Give two examples of weighted code. (2)

(c) Perform the following subtraction using the 10's complement arithmetic 196-155. (2)

(d) Design XNOR gate using minimum number of NAND gates only. (3)

UNIT - II

Q4. (a) Design BCD-to-Excess -3 code converter. (4)

(b) Reduce the following Boolean expression using Boolean algebra

((AB' + ABC) +A(B+AB'))' (3)

(c) Design a 3 bit binary-to-octal decoder. (3)

OR

Q5. (a) Design a combinational circuit with 4 input and outputs. The output generates the 2's complement of the input binary number. (5)

(b) Using the K-map simplify the following function into minimal SOP

$f(u,w,x,y,z) = \sum m(0,2,5,7,9,11,13,15,16,18,21,23,25,27,29,31)$ (5)

UNIT - III

Q6. (a) Explain the working of Master Slave J-K Flip-Flop. (5)

(b) How will you convert a D flip flop into a J-K flip flop. (5)

OR

Q7. (a) Describe the working of shift left register with diagram. (3)

(b) Design a synchronous decade counter to count in the Excess-3 code sequence. Using minimum number of J-K flip flops. (7)

UNIT – IV

Q8. (a) Explain the working of R-2R digital-to-analog converter. Discuss the characteristics of D\A converters. (6)

(b) What is PLD? How are PLD s categorized? Draw the structure of simple PLA of the following function

X = A'B'C'D + A'B'CD

Y = A'B'CD + ABCD'

Z = A'B'C'D + A'B'CD + ABCD' (4)

OR

Q9. (a) Draw the functional block diagram of 8085 microprocessor. (7)

(b) Write short notes on **Any One** of the following: (3)

(i) Content addressable memory

(ii) 3-bit parallel comparator A/D converter

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